Customer No.: 31561
Application No.: 10/711,533
Docket No.: 13791-US-PA

AMENDMENTS

To the Claims:

Please amend claims as follows.

Claim 1. (Currently amended) A method of fabricating a capacitor, comprising:

forming a dielectric layer on a semiconductor substrate;

forming an upper electrode on the dielectric layer, the upper electrode having a plurality of opening therein;~~and~~

performing a doping step to the semiconductor substrate through the openings to form a single doped region as a lower electrode in the semiconductor substrate under the upper electrode~~.~~; and

forming a plurality of metal silicide layers on portions of the single doped region within the openings.

Claim 2. (Original) The method of claim 1, wherein the doping step comprises a tilt ion implantation process.

Claim 3. (Original) The method of claim 1, wherein the doping step comprises:

conducting a substantially vertical ion implantation process to form a plurality of doped regions in the substrate under the openings; and

conducting an annealing process to make the doped regions merge into the single doped region.

Claim 4. (Original) The method of claim 1, wherein the step of forming the upper electrode on the dielectric layer comprises:

forming a conductive layer on the dielectric layer; and

patterning the conductive layer into the upper electrode with a lithography process and an etching process.

Claim 5. (Original) The method of claim 1, wherein the upper electrode includes a plurality of bar-like conductive layers connecting with each other, and the openings in the upper electrode are trench-like openings between the bar-like conductive layers.

Claim 6. (Original) The method of claim 5, wherein the upper electrode has a comb-like structure or a fishbone-like structure.

Claim 7. (Original) The method of claim 1, wherein the upper electrode has a net-like structure.

Claim 8. (Original) A method of fabricating a capacitor, comprising:

forming a dielectric layer on a silicon substrate;

forming an upper electrode on the dielectric layer, the upper electrode comprising doped polysilicon and having a plurality of opening therein;

performing a doping step to the substrate through the openings to form a single doped region as a lower electrode in the substrate under the upper electrode;

forming a spacer on a sidewall of each opening in the upper electrode; and

performing a self-aligned silicide (salicide) process to form a plurality of metal silicide layers on the upper electrode and portions of the single doped region within the openings.

Claim 9. (Original) The method of claim 8, wherein the doping step comprises a tilt ion implantation process.

Claim 10. (Original) The method of claim 8, wherein the doping step comprises:

conducting a substantially vertical ion implantation process to form a plurality of doped regions in the substrate under the openings; and

conducting an annealing process to make the doped regions merge into the single doped region.

Claim 11. (Original) The method of claim 8, wherein the step of forming the upper electrode on the dielectric layer comprises:

forming a conductive layer on the dielectric layer; and

patterning the conductive layer into the upper electrode with a lithography process and an etching process.

Claim 12. (Original) The method of claim 8, wherein the upper electrode includes a plurality of bar-like conductive layers connecting with each other, and the openings in the upper electrode are trench-like openings between the bar-like conductive layers.

Claim 13. (Original) The method of claim 12, wherein the upper electrode has a comb-like structure or a fishbone-like structure.

Claim 14. (Original) The method of claim 8, wherein the upper electrode has a net-like structure.

Claim 15. (Original) The method of claim 8, wherein the metal silicide layers comprise a silicide of a refractory metal.

Claim 16. (Original) The method of claim 15, wherein the refractory metal is selected from the group consisting of Ti, W, Pt, Co and Ni.

Claim 17. (Original) A method of fabricating a capacitor, comprising:

forming a dielectric layer on a silicon substrate;

forming an upper electrode on the dielectric layer, the upper electrode comprising doped polysilicon and having a plurality of opening therein;

performing a doping step to the substrate through the openings to form a single doped region as a lower electrode in the substrate under the upper electrode;

forming a liner layer on a sidewall of each opening in the upper electrode;

forming a spacer on each liner layer on a sidewall of an opening;

removing the spacer; and

performing a self-aligned silicide (salicide) process to form a plurality of metal silicide layers on the upper electrode and portions of the single doped region within the openings.

Claim 18. (Original) The method of claim 17, wherein the doping step comprises a tilt ion implantation process.

Claim 19. (Original) The method of claim 17, wherein the doping step comprises:

conducting a substantially vertical ion implantation process to form a plurality of doped regions in the substrate under the openings; and

conducting an annealing process to make the doped regions merge into the single doped region

Claim 20. (Original) The method of claim 17, wherein the step of forming the upper electrode on the dielectric layer comprises:

forming a conductive layer on the dielectric layer; and

patterning the conductive layer into the upper electrode with a lithography process and an etching process.

Claim 21. (Original) The method of claim 17, wherein the upper electrode includes a plurality of bar-like conductive layers connecting with each other, and the openings in the upper electrode are trench-like openings between the bar-like conductive layers.

Claim 22. (Original) The method of claim 21, wherein the upper electrode has a comb-like structure or a fishbone-like structure.

Claim 23. (Original) The method of claim 17, wherein the upper electrode has a net-like structure.

Claim 24. (Original) The method of claim 17, wherein the metal silicide layers comprise a silicide of a refractory metal.

Claim 25. (Original) The method of claim 24, wherein the refractory metal is selected from the group consisting of Ti, W, Pt, Co and Ni.

Claim_26. (New) The method of claim 1, wherein forming a plurality of metal silicide layers on portions of the single doped region within the openings comprises steps of:

forming a spacer on a sidewall of each opening in the upper electrode; and

performing a self-aligned silicide (salicide) process to form a plurality of metal silicide layers on the upper electrode and portions of the single doped region within the openings.